The Silicon tracker developments at KEK

19 Dec. 2007
Toru Tsuboyama (KEK)
For Belle vertex detector collaboration
and
SOIPIXEL collaboration at Torino, Italy
Outline

• Topics from KEK
• Upgrade plan of the silicon vertex detector.
• SOI pixel sensor activity
• Synergy with the ILC detector R&D.
News from KEK

• KEK director general decided to upgrade KEKB factory to a $2\times10^{35}$ /cm$^2$/s machine.
  – The current KEKB will be shutdown at end of 2008 and the commissioning of the new KEKB will happen in 2012.

• A 3 GeV electron test beam line, using KEKB electron beam, has started October 2007.

• J-PARC: Commissioning of the 3-GeV radiofrequency-synchrotron was successfully done in November.

• **R&D of ILC accelerator and detector will be continued independent of KEKB upgrade and JPARC.**
RCS 3GeV加速成功
2007年10月31日 14時03分23秒

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A new electron beam line

• Extract the bremsstrahlung $\gamma$ from KEKB electron ring (8 GeV) and convert into $e^+e^-$ pairs and transferred to the experiment area using five bending and four Q magnets.

• Started operation in October 2007.

• Beam intensity is not enough. (Low rate test can be done.)

• Coordinator: T.Kawasaki  kawasaki@hep.sc.niigata-u.ac.jp

- Beta-SVD upgrade
- JPARC scintillation fiber
- ILC calorimeter
- Wire chamber R&D
Upgrade plan of Belle silicon vertex detector

- 1.5 T solenoid
- Central tracking chamber
- CsI calorimeter
- 3.5 GeV e\(^{+}\) beam
- 8 GeV e\(^{-}\) beam
- 3.5 GeV e\(^{+}\) beam
- Aerogel Cerenkov
- Time of flight
- K\(_{L}\) and \(\mu\) counter
- Silicon Vertex Detector

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Silicon Vertex Detector

• SVD reconstructs two vertices of B decay.
  – B flight length ~ 200 µm.
• The CP violation parameters are extracted from the distribution of distance between two vertices.

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KEKB upgrade plan

- The CP violation in framework of the Standard model has been established.
- To explore the physics beyond the standard model we need more luminosity.
- Many new phenomena would appear around $50 \text{ ab}^{-1}$.
- There are several scenarios to achieve this luminosity goal.
Upgrade of the vertex detector

• Configuration
  – Six layers: for reconstruction of low-momentum tracks.
  – Better vertex resolution.
  – Material inside acceptance must be minimized.

• Sensor options
  – DSSD
  – Pixel

• Readout electronics
  – 10KHz trigger rate
  – Hit occupancy should be kept <10%
Consideration of the inner most layer (I)

- Two layers DSSD:
  - 20% improvement at high momentum thanks to the smaller detector radius.
  - Robust hit finding under background.
- Monolithic Pixel:
  - Similar performance and robust tracking
  - R&D in progress

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Sensor configuration

- **Belle acceptance:** $17^\circ < \theta < 150^\circ$
- **Outer radius:** 150 mm
- **Inner radius:** 13 mm
  - Beam pipe ($r = 10$ mm)
  - For better vertex resolution.
- **Total sensitive area:** $\sim 1 \text{ m}^2$
- **Inclined ladders in Layer 5 and 6**
- **Material budget**
- **Ladder lengths:** (75 cm / bar, 60 cm)
- **Option in Layer 1 sensor**

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### Parameters

<table>
<thead>
<tr>
<th>Parameter</th>
<th>p</th>
<th>n</th>
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<tbody>
<tr>
<td>Sensitive area (mm²)</td>
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<td>Strip length (mm)</td>
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<td>Strip pitch (µm)</td>
<td>25.5 (p)</td>
<td>51 (n)</td>
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<td>Readout pitch (µm)</td>
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<td>51 (n)</td>
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<tr>
<td>Num. of readout ch.</td>
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<td>1024</td>
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<tr>
<td>Bias resistor (MΩ)</td>
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</tr>
</tbody>
</table>

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Evaluation of striplet sensor

- Leakage current
  0.09 µA=16nA/cm² @ 80V / 25°C

- Laser scan with VA1TA
  - Reasonable charge separation on p-side and n-side

- Beam test with APV25
  - Full depletion voltage ~65 V
  - S/N ~25(p side)/27(n side ) for MIP
High-density kapton flex circuits

• Stripllet readout: 1024 signals in 10 mm width.
• A 2-layer 38 µm pitch design is chosen.
• A sub company of CASIO produces the kapton flex circuit in the semiconductor-level clean rooms.
  – High yield.
  – Cost is low in mass production.

• Issues
  – Size is limited to 8x14 cm.
  – Tin plating only. Gold plating outside of CASIO reduces the production yield.
  – We are not very welcomed. Our order interferes their mass production.
Readout with APV25 ASIC

- APV25 is chosen
  - Originally developed for CMS Silicon tracker
- Operated with 40MHz clock
  - 192 stage pipeline (~4 µsec trigger latency)
  - Up to 32 readout queues
  - 128 ch analog multiplexing (3 µsec@40 MHz)
  - Dead time: negligible at expected trigger rate of 10 kHz

Noise = \((246 + 36/pF) \) @50nsec

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Hit timing reconstruction

- B-Factory --> 2 nsec bunch crossing
  - APV25 deconvolution filter can not be used.
- Hit time reconstruction
  - Proposed by Vienna group
  - Read out 3, 6 ... slices in the pipeline for one trigger.
  - Extract the hit timing information from waveform.

Proven in beam tests: Resolution ~ 2 nsec.
Reconstruction done in the FPGA chips in FADC board.

(HEPHY Vienna)
APV25 Readout

- APV25 is readout with simplest hardwares.
  - No optical fiber, No support chips.
  - Readout electronics were developed from scratch.
- Hybrid (Princeton):
  - Mounted with four APV25 chips only.
  - Signals are transferred to the repeater system with 2m copper twisted cable.
- Repeater (Vienna):
  - Double sided readout.
  - Floating LVPS. LVPS are floated to the bias voltage in P-side and N-side order to minimize the effect of pin holes in the AC coupling.
- FADC (Vienna):
  - 9UVME size. Each board readouts 6 hybrids (24 channels)
  - FADC + Data sparsification + hit-time reconstruction on FPGA
- Interface to DAQ (Cracow)
  - Data from FADC board is transferred to the event builder.
Test bench of APV25 (APVDAQ)

• Developed by HEPHY (Vienna) for adaptation test of APV25 in Belle.
  – Operated with various APV25 modes
  – External and internal trigger.
  – Evaluations: test-pulse, radiation source, IR pulse laser and test beam line.

• Hardware:
  – VME board (Control / FADC)
  – AC coupled Repeater
  – Four-chip Hybrid

• Software
  – GUI version (NI “Lab Windows”)
  – C / Linux version (developed with Princeton group)

Beam tests
2005.04 --- Evaluation of striplet sensor readout with APV25
2005.12 --- Evaluation of DSSD for the SVD upgrade (APV25+VA1 readout mixed)
2007.11 --- Evaluation of new readout system for Belle SVD upgrade.
April 2005

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Dec. 2005

- Almost the last beam test at the KEK proton synchrotron.
- APV25 and VA1 ladders
- Test of the new sensor for Belle upgrade.
Nov. 2007

• The first experiment at the KEK new beam line.

• Demonstration of the new DSSD sensor, hybrid, repeater and FADC. Six hybrids were readout successfully.

• CM subtraction by FPGA is tried.
Mount readout chips on DSSDs

- In order to avoid the long (up to 56 cm) kapton flex, Vienna group proposed to mount the readout chips on DSSD sensors.
  - Capacitance due to long kapton flex can be avoided.
  - Detail resolution study including material budget and S/N is necessary.
  - Various cooling method will be tried. (Air, water channel …)
Progress of the SOIPIX project

• OKI 150 nm process (200 nm since this year)
• Normal CMOS process.
• 2005/2006 Experimental line (150 nm)
• 2007 Mass production line (200 nm)

• Team leader: Y. Arai  yasuo.arai@kek.jp
OKI SOI structure

- Add a few steps to the normal CMOS production.
  - Remove the buried oxide (BOX) where implant is done.
  - Implant the P/N type ions.
  - Fill the hole with SiO2 and annealing.
  - Make a via for the contact to metal 1.
  - Fill the via with plug metal.

- Normal CMOS process will be continued.
Progress of the SOIPIX project

- 2005 First submission (150 nm)
- 2006 Second submission (150 nm)
- 2007 Third submission in preparation (200 nm)
Readout with COBI system

- COBI: General purpose FPGA board including FADC and USB interface developed by Hawii Univ. HEP group.
- 128x128 pixel chip is evaluated with COBI.
- FADC data is stored in the FIFO in the FPGA and transferred to PC via USB interface.
- Response to light is measured. DAQ rate: 1Frame = 40 msec.
- **Beam test will be done in next February.**

![Diagram of COBI system interface]

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Response to room light

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Synergy with ICL

19 Dec 2007
Toru Tsuboyama (KEK)
Function of the vertex detector in B factories

(I)

• Basic design of Belle/Babar silicon vertex detectors is valid in Super B factories.
  – Even at 100 times larger luminosity, B factories are forever low-energy machines.

• Measure the decay vertices of the two B mesons, especially in the Z direction.
  – At Y(4S) energy, the events are either a pure BB system or non-B events.
  – If a B decay mode is identified, the other tracks and energy clusters belong to the other B.
  – Thanks to the long lifetime and slow $B^0$-$B^0$ oscillation, the resolution of the silicon vertex detector is adequate.
Function of the vertex detector in B factories (II)

- Help the tracking by the central drift chamber
  - Extend the lever arm of high-pt tracks for $B \to K\pi$, $\pi\pi$ etc.
  - The detection of slow $\pi$ in $B \to D^*X \to D\pi sX$.

- $K_s$ reconstruction in $B \to K(*) \gamma$.
  - Only 2 charged tracks appears separated from $B$ decay vertex.
  - Larger radii of outer 2 layers increase the $K_s$ acceptance.
Sensor production

• Double-sided sensor is essential to minimize the material.
• 300 µm is acceptable. The thinner the better.
• Mass production starts in 2009.
• HPK stopped the double-sided production line.
• We have started to find other suppliers.
Alignments

- Ambiguities of alignment between sensor and sensor, and, between silicon vertex detector and central drift chamber are \(O(10 \, \mu m)\), in case of present Belle.
  - We guess the field non-uniformity due to final-focus magnets prevents better alignment with magnet.

- Above 5 ab\(^{-1}\) integrated luminosity (x7 of the present Belle data), statistics error of B decay vertex measurement reaches this level.
  - Physics output will be limited by sensor alignment ambiguity.

- Need absolute detector alignment methods.
Material thickness

- Beam energy of a Super B factory is essentially the same as the existing machines.
- Material in silicon vertex detector should be kept or decreased for a better performance of the whole system.
- IP chamber should hold beam current (a few Ampere).
  - A vacuum chamber thickness with liquid cooling is necessary.
  - Extremely thin silicon sensors will not improve the vertex resolution.
- Readout hybrid should be placed outside the detector acceptance.
- If ASIC is put on the sensor, cooling material will be the next issue. (Air cooling and high-temperature should be tried.)
- R&D of monolithic pixel sensor is active in Belle /
Structure and Infrastructures

• KEKB adopted High-current options.
  – Backgrounds from beam increase accordingly.
    • Short shaping-time
    • Pipelined readout is necessary.
• Outer radius will be larger.
• Readout channel will be 4-10 times than that of the present system.
• Cable, cooling, position of the readout ASICs requires more space for the vertex detector.
• BKG simulation group is designing the Belle structure with more background shield around the silicon tracker region.
• Solution: Low-material and stable support and cooling system, low power ASIC will allow realistic detector design.
ASIC design

• Train structure is completely different
• ILC --- 1 msec train / 200 msec period.
• KEKB---- DC beam (2 nsec crossing) .
  – Electronics should be always active.
  – Cooling : If ASIC should be mounted on DSSD sensors, low mass cooling system should be developed.
Summary of this talk

• KEK decided to upgrade the KEK B factory. Luminosity goal depends on budget.

• Conceptual design exists for the SVD upgrade.
  – No detailed designs yet.

• KEK SOIPIXEL collaboration in progress.
  – 2007 OKI MPW will be submitted in 1-2 weeks.